Modeling and Design of GaAs MESFET Control Devices for Broad-Band Applications

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Abstract—**In this paper, closed-form expressions are developed for the small-signal parameters of broad-band GaAs control MESFET's. The theoretical conducting-state resistance and nonconducting-state capacitance are compared with experimental data and demonstrate the usefulness of the models. Additionally, we considered the power handling capability of these devices and describe the various limitations in both conducting and nonconducting states. Our models show that self-aligned gate devices (SAGFET's) have a broad-band cutoff-frequency figure of merit as much as twice that of conventional MESFET's, although the voltage handling capability of the SAGFET is considerably inferior.**

NOMENCLATURE

a^*	Thickness of the channel below the gate metal.
a_{ds}	Depletion region thickness due to the free-surface potential.
a_{dm}	Depletion region thickness due to the metal–semiconductor junction.
C_{nc}	Nonconducting-state total equivalent capacitance.
C_i	Intrinsic capacitance in the conducting state between gate and channel.
C_{igs}	Intrinsic capacitance in the nonconducting state between gate and source.
C_{igd}	Intrinsic capacitance in the nonconducting state between gate and drain.
C_{isd}	Intrinsic source-to-drain capacitance (used for self-aligned-gate devices).
C_{egs}	Extrinsic capacitance in either state between gate and source.
C_{egd}	Extrinsic capacitance in either state between gate and drain.
C_{esd}, C'_{esd}	Extrinsic capacitance in the nonconducting state between drain and source, through the GaAs and through air respectively.
C_{gs}, C_{gd}	Equivalent gate-to-source and gate-to-drain capacitance respectively.
$K(k)$	Complete elliptic integral of the first kind.
F_{cs}	Broad-band cutoff frequency figure of merit.
L_{gd}	Distance between gate metal and drain metal.
L_{gs}	Distance between gate metal and source metal.
L_{sd}	Distance between source metal and drain metal.
L_g	Gate length.
L'_{gd}	For structure B the distance between the drain deep n^+ contact and the edge of the recess depth; for structures A and D the distance between drain n^+ deep contact and the metal gate; and for structure C the distance between drain metal and the edge of the recess.
L'_{gs}	For structure B the distance between source deep n^+ contact and edge of the recess depth; for structures A and D the distance between source n^+ deep contact and metal gate; for structure C the distance between source metal and edge of the recess.
L'_g	Adjusted gate-length L_g to include recess extensions; same as L_g for structures A and D.
L_s, L_d	Length of source and drain metallizations respectively (assumed to be equal).
L'_s, L'_d	Adjusted length of source and drain metallization respectively (see Fig. 2).
q	Electron charge (positive).
R_c	Total conducting-state resistance.
R_{cc}	Contact resistance for metal-to-n^+ interface.
R_{c0}	Contact resistance due to metal-to-n^+ interface and n^+ deep contact layer.
R_{bias}	Resistance in series with the gate.
r_d	Recess depth.
R_p	Conducting-state nonchannel resistance.
R_{p1}	Parasitic resistance with n^+ surface layer (see the Appendix).
R_{ch}	Conducting-state channel resistance.
R_{gd}	Resistance between the drain contact and the channel.
R_{gs}	Resistance between the source contact and the channel.
t_{ds}	Depletion region thickness in the heavily doped surface layer due to the surface potential.
t^*	Surface n^+ layer thickness.
V_p	Magnitude of the applied voltage to pinch-off the channel.
V_{bias}	Magnitude of the dc voltage at the gate.
W	Gate width of the MESFET.
ρ	Resistivity of the channel region.

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ρ_+ Resistivity of the heavily doped region (assumed to be 2.5×10^{-3} $\Omega\cdot$cm).
ϵ_0 Permittivity of free space.
ϵ Permittivity of GaAs.

I. Introduction

During the past few years, considerable work has been done on designing and manufacturing control components using GaAs MESFET devices. This increased interest is attributed to improvements in GaAs processing technology and the attractive features of GaAs MESFET switches (such as low bias power, fast switching speed, MMIC compatibility, and broad-band capabilities). The MESFET used as a passive control device is basically a voltage-controlled resistor whose value is determined by the dc bias voltage applied at the gate of the device. For most control applications, the MESFET is switched between a low-impedance, or conducting, state and a high-impedance, or nonconducting, state, corresponding to the linear and the cutoff regions of the FET characteristics respectively. At frequencies of most interest (below 30 GHz) the conducting state source-to-drain impedance is mostly resistive while in the nonconductive state the impedance is mostly capacitive.

Earlier work has identified the conducting state resistance, R_c, and the nonconducting state capacitance, C_{nc}, as the key equivalent circuit elements used in characterizing broad-band MESFET switches [1], [2]. Based on R_c and C_{nc} the broad-band cutoff frequency figure of merit can be defined as

$$F_{cs}=\frac{1}{2\pi R_c C_{nc}}. \tag{1}$$

In this paper the design considerations for GaAs control MESFET's (particularly for broad-band applications) are evaluated, and future performance capabilities are examined. The paper is organized as presented below.

In Section II, equivalent circuit parameters for the two states of the MESFET control device are developed for the four different device structures shown in Fig. 1. Device structure A is a planar device, B is a gate recessed structure, C is a gate recessed structure with a surface n^+ layer and D is a self-aligned-gate FET (SAGFET). In Section III the power handling capability of MESFET control devices is described. In Section IV a variety of previously reported discrete device characteristics are compared to the modeled parameters. In addition, a dual 2-throw component is evaluated under both low and high power conditions. In Section V, the various device structures are compared.

II. Modeling of Equivalent Circuit Parameters

In this section the resistances and capacitances are modeled from first principles in such a manner that closed-form analytical equations can be derived. Since our focus is mainly on the effect of the geometrical shape of the MESFET on the values of the equivalent circuit elements, we assume uniform doping profiles throughout.

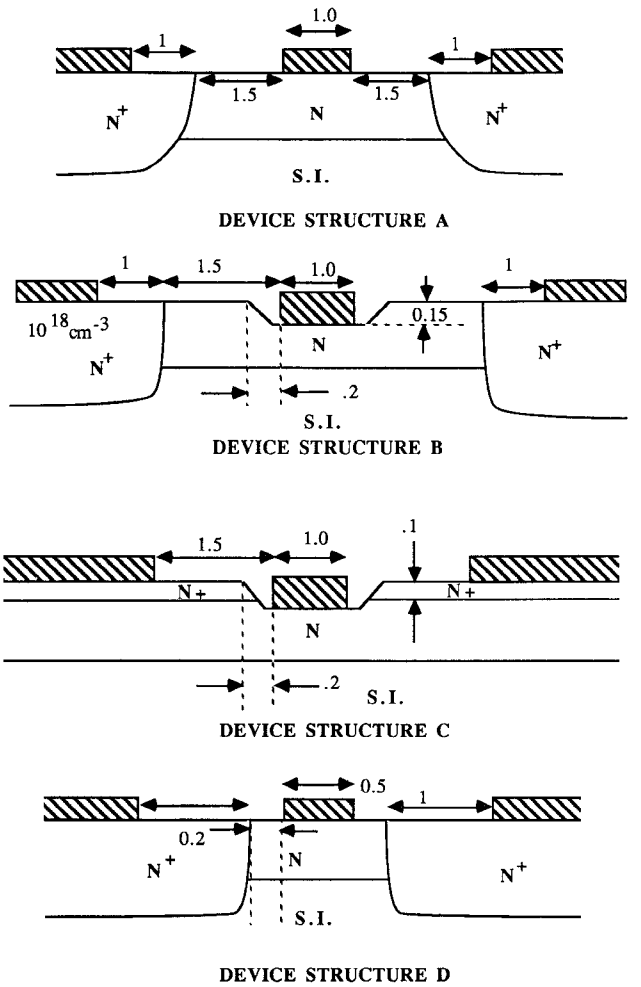


Fig. 1. The MESFET device structures (with typical dimensions). All dimensions are in microns. The N^+ doping is 10^{18} cm^{-3}.

A. Resistance Modeling

For control applications, the conducting-state resistance of the MESFET device can be subdivided into the channel resistance, R_{ch}, and the parasitic resistance, R_p. The channel resistance must be small in the conducting state, while in the nonconducting state the channel is fully depleted so that the channel resistance is very large and relatively unimportant (capacitive impedances dominate in the nonconducting state).

The parasitic resistance is the combination of the metal-to-semiconductor contact resistance and the resistance of the semiconductor between the contacts and the channel. With recessed gate technology and practical device dimensions, the contact resistance R_{c0} is usually negligible. Thus, we initially neglect any contact resistance and reintroduce this contribution later in considering short gate SAGFET's where the contact resistance becomes important.

The conducting-state resistance of structure A is relatively simple to calculate. Including the surface depletion due to the free-surface pinning voltage and the gate-metal

to channel depletion, the resistances are given as

$$R_{gd} = \frac{\rho L'_{gd}}{W(a^* - a_{ds})} \tag{2}$$

$$R_{gs} = \frac{\rho L'_{gs}}{W(a^* - a_{ds})} \tag{3}$$

$$R_{ch} = \frac{\rho L'_{g}}{W(a^* - a_{dm})}. \tag{4}$$

For structure B the parasitic resistance (i.e, resistance other than the channel resistances) can be calculated by approximating the inclined recess edge as an abrupt edge. A further approximation of assuming an equipotential surface at the edge of the abrupt recess permits separation of the parasitic and the channel resistances. By including the depletion due to the free-surface pinning and the gate-to-channel built-in voltage and using conformal mapping [3], the parasitic resistances of structure B are given by

$$R_{gd} = \frac{\rho}{W}\left\{\frac{L'_{gd}}{a^* + r_d - a_{ds}} + \frac{2}{\pi}\ln\sec\left[\frac{\pi}{2}\left(\frac{r_d - a_{ds} + a_{dm}}{a^* + r_d - a_{ds}}\right)\right]\right\} \tag{5}$$

$$R_{gs} = \frac{\rho}{W}\left\{\frac{L'_{gs}}{a^* + r_d - a_{ds}} + \frac{2}{\pi}\ln\sec\left[\frac{\pi}{2}\left(\frac{r_d - a_{ds} + a_{dm}}{a^* + r_d - a_{ds}}\right)\right]\right\} \tag{6}$$

while R_{ch} is given by (4).

Structure C was approximated by distributed resistance networks since the surface n^+ layer has much smaller resistance than the n channel. The resistance components for this structure is derived in the Appendix, with the parasitic resistances given as

$$R_{gd} = \frac{R\|r}{K}\left[\left(\frac{r}{R} + \frac{R}{r}\right)\coth KL'_{gd} + \frac{2}{\sinh KL'_{gd}}\right] + L'_{gd}(r\|R) \tag{7}$$

and

$$R_{gs} = \frac{R\|r}{K}\left[\left(\frac{r}{R} + \frac{R}{r}\right)\coth KL'_{gs} + \frac{2}{\sinh KL'_{gs}}\right] + L'_{gs}(r\|R) \tag{8}$$

where

$$r = \frac{\rho_+}{W(t^* - t_{ds})} \tag{9}$$

$$R = \frac{\rho}{W(a^* - a_{dm})} \tag{10}$$

$$G = \frac{W}{\rho(r_d + a_{dm} - t^*)} \tag{11}$$

$$K = \sqrt{G(R + r)} \tag{12}$$

and R_{ch} is given by (4).

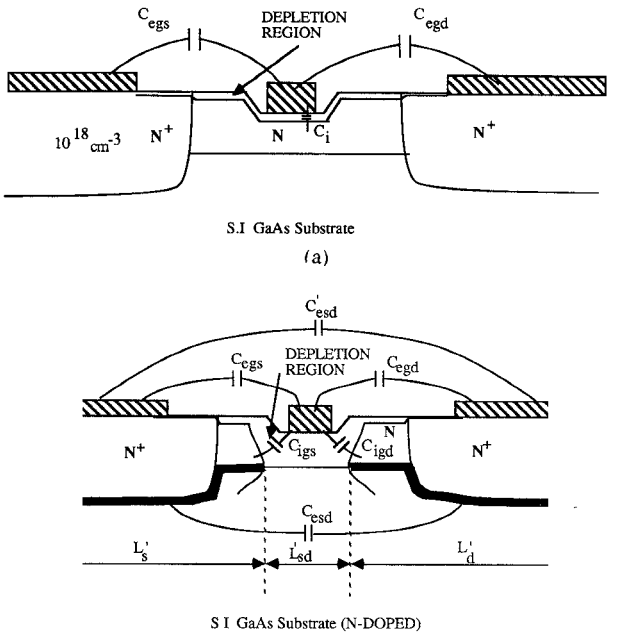


Fig. 2. Origin of the capacitances for the two states of the MESFET control device. (a) Conducting state. (b) Nonconducting state.

Calculations of the resistance for device structure D follow that of structure A, except that the n^+ deep contact and metal contact resistances have to be included. An upper bound for the contact resistance can be found by assuming that the n^+ contact layer thickness is the same as the channel thickness. Neglecting surface depletion effects and the discontinuities in the geometry of the film at the n^+–n contact, the total contact resistance is approximately given as (see [3, eq. (12)])

$$R_{c0} = R_{cc} + \frac{\rho_+}{W}\left(\frac{L_{gd} - L'_{gd} + L_{gs} - L'_{gs}}{a^*} + 0.882\right) \tag{13}$$

assuming that $3a^* < (L_{gd} - L'_{gd}), (L_{gs} - L'_{gs})$. We assume ρ_+ to be $2.5 \times 10^{-3}\ \Omega\cdot$cm, which corresponds to a doping of about $10^{18}\ \text{cm}^{-3}$.

B. Capacitance Modeling

The device capacitance can also be subdivided into two components: the intrinsic Schottky gate depletion layer capacitance and the extrinsic parasitic coupling capacitance. Fig. 2(a) shows the physical origin of the various important capacitances in the conducting state. The capacitance C_i is the intrinsic capacitance with the gate at zero bias, and is given by

$$C_i = \frac{\epsilon L_g W}{a_{dm}}. \tag{14}$$

The important extrinsic capacitances in the conducting state are the source and drain metal coupling to the gate metal in the region above the GaAs. These can be calculated for two planar parallel plates as in Smythe [4], neglecting any effect of the gate recess and finite metal

thickness, with the results given as

$$C_{egd} \quad \text{or} \quad C_{egs} = \epsilon_0 W \frac{K(\sqrt{1-k^2})}{K(k)} \tag{15}$$

where for C_{egd}

$$k = \sqrt{\frac{L_{gd}}{L_{gd}+L_g}} \tag{16}$$

when $L_s, L_d \gg L_g$, while for C_{egs},

$$k = \sqrt{\frac{L_{gs}}{L_{gs}+L_g}} \tag{17}$$

when $L_s, L_d \gg L_g$.

The nonconducting-state capacitances are shown in Fig. 2(b). The intrinsic capacitances with structures A–C [5] are given as

$$C_{igd} \quad \text{or} \quad C_{igs} = \epsilon W \tan^{-1} \sqrt{\frac{V_p + 0.8}{V_{\text{bias}} - V_p}} \tag{18}$$

while for structure D the calculation is approximated for two different depletion conditions: first, the gate depletion region not extending throughout the conducting channel and second, the gate depletion region extending throughout the conducting channel. In the first case the capacitance can be estimated by (18) and the second case can be approximated by

$$C_{isd} = \frac{\epsilon a^* W}{(L_g + L'_{gd} + L'_{gs})}. \tag{19}$$

This approximation results in a source-to-drain intrinsic capacitance equal to that obtained without a gate contact. For the SAGFET devices shown in Fig. 1, (19) was used with channel doping densities less than 0.5×10^{17} cm^{-3} while (18) was used for higher channel doping densities. A more exact approach which solves Laplace's equation with mixed boundary conditions was considered unnecessary since the extrinsic capacitance dominates in practical structures.

The extrinsic capacitance in the nonconducting state consists of three components. The first is attributed to the source and drain coupling to the gate in the region above the GaAs and is given by (15)–(17). The second component is the extrinsic capacitance that couples through the S.I. substrate, namely the substrate source-to-drain coupling capacitance, and is given as

$$C_{esd} = \epsilon W \frac{K(\sqrt{1-k^2})}{K(k)} \qquad k = \sqrt{\frac{(2L'_s + L'_{sd})L'_{sd}}{(L'_s + L'_{sd})^2}} \tag{20}$$

for a symmetric device, where L'_{sd} is the distance between the nondepleted channel at the S.I. interface as shown in Fig. 2(b). The third component is the extrinsic capacitance that couples through the air, namely the metallic source-to-drain coupling capacitance C'_{esd} and is given by (20) with L'_{sd} replaced by L_{sd}, L'_s by L_s, and ϵ by ϵ_0. In addition, increased capacitances can result which depend upon the FET layout.

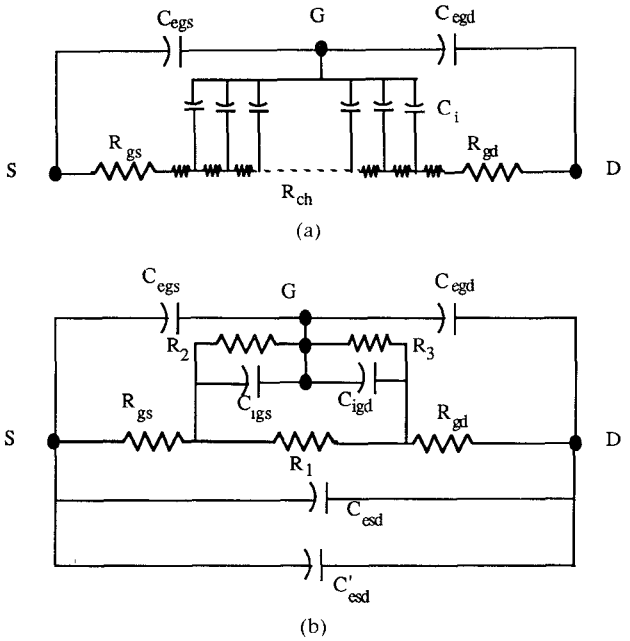


Fig. 3. The RF equivalent circuit on the control MESFET in the two states. (a) Conducting state. (b) Nonconducting state.

C. Equivalent Circuits for the Two States

The modeled capacitances and resistances can be combined to form small-signal equivalent circuits that would represent the two states of the MESFET control device. The conducting-state equivalent circuit is shown in Fig. 3(a), which includes a distributed model of the intrinsic capacitance and channel resistance. This extension helps explain some of the broad-band power-handling behavior, as shown in Section III.

The nonconducting-state equivalent circuit is shown in Fig. 3(b). While R_{gs} and R_{gd} are bias voltage dependent, it is sufficient to assume constant values for most applications. The components of channel resistance (i.e., between source and drain, between source and gate, and between drain and gate) are extremely large (>100 k$\Omega \cdot$mm) and process dependent. Although the specific values can be important at very low frequency, it is usually sufficient to assume arbitrarily large values.

III. Power Handling Considerations

Power handling capability of a control device is usually characterized by either the power level for 1 dB deviation from linear behavior or the total harmonic distortion (THD). Although for narrow-band applications a single figure of merit [6] is sufficient, for broad-band applications both the maximum current handling capability in the conducting state and the maximum voltage handling capa-

bility in the nonconducting state need to be considered, as the circuit impedance level is constrained to 50 Ω.

For a broad-band GaAs MESFET switch, the power handling is also dependent on the gate bias circuitry. The gate is usually biased with a large gate bias resistance (ranging from 1 to 10 kΩ) because such a scheme can be easily implemented in a MMIC. Before analyzing the details of the power limitation with such a gate bias circuit, the various electrical power limiting mechanisms that are present in a MESFET control device will be discussed (thermal design considerations will not be treated).

In the conducting state there are three mechanisms that can be important in determining the power limitations of the MESFET control device, namely the current limitation with a floating gate, forward current injection during part of the RF cycle, and premature current saturation when the gate is not floating. When the gate is floating (i.e., high frequency so that the gate-to-channel capacitive impedances are much less than the gate bias resistance), the maximum channel current is determined by the maximum current a floating gate may allow. This value may be limited by pinch-off or open channel capacity, depending on the relative lengths of the gate and the channel and the pinch-off voltage. Additionally, forward injection may occur because one side of the gate becomes forward biased. Since the large bias resistance limits the gate current flow, forward current injection is usually unimportant in limiting power capability. When the gate is not floating, the gate voltage remains relatively unchanged as the applied RF voltage increases. As a result, the RF voltage in the channel will tend to put the device either into premature saturation or forward bias.

In the nonconducting state, there are two mechanisms that can be important in determining the power limitations. When a RF voltage is applied across a nonconducting MESFET, a voltage difference develops between the source and the drain. With the gate capacitively coupled, one junction becomes closer to breakdown, while the other junction becomes closer to a partially opened channel during half of the RF cycle. Our experience indicates that the nonconducting state does not introduce large distortions at the output when one of the junctions goes into breakdown, since the large gate bias resistance limits the gate current pulse.

Fig. 4 shows four different MESFET control device configurations that are commonly encountered in control circuits. Fig. 4(a) shows a conducting-state series-mounted control device configuration which is matched. At high frequencies ($f \gg 1/2\pi C_{gs}R_{\text{bias}}$ or $1/2\pi C_{gd}R_{\text{bias}}$), the channel signal is capacitively coupled onto the gate; as a result, the maximum current is equal to the current handling capability of a floating gate device. However, at low frequencies the RF voltage at the gate is "shorted" to ground. Therefore, in the positive-going channel-voltage cycle, the gate is reversed biased and depleted. Increasing RF voltage would take the control device into the current saturation region as shown in Fig. 4(a). In the negative-going channel-voltage cycle the gate is forward biased, and

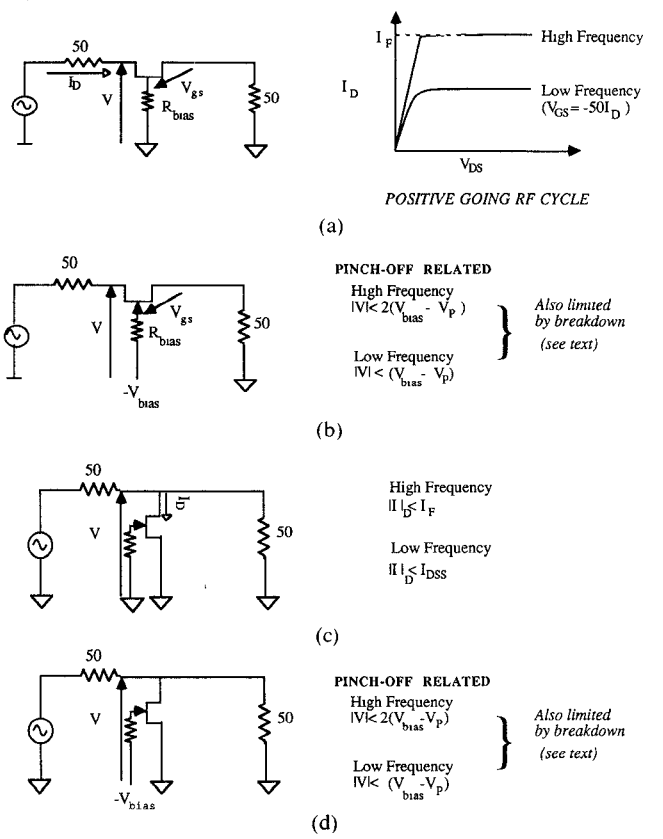


Fig. 4. Large-signal power handling limitations. (a) Current limitations of a conducting-state series-mounted control device. (b) Voltage limitations of a nonconducting-state series-mounted control device. (c) Current limitations of a conducting-state shunt-mounted control device. (d) Voltage limitations of a nonconducting-state shunt-mounted control device.

as a result injection from the gate into the channel occurs. This forward current injection from the gate is expected to be about ($R_{\text{bias}}/50$ Ω) smaller in amplitude than the output signal at the matched load, and is usually negligible.

Fig. 4(b) shows a nonconducting-state series-mounted MESFET control device. Based on the arguments given above (also see Ayasli [2]) it is seen that a symmetric device comes out of pinch-off when $|V| \gtrsim 2(V_{\text{bias}} - V_p)$ at high frequencies and $|V| \gtrsim V_{\text{bias}} - V_p$ at low frequencies, where V is the peak RF signal voltage at the drain. As mentioned earlier, single junction breakdown is unimportant when R_{bias} is large enough to keep the current injection low. In situations where slight nonlinearities are acceptable, V_{bias} may be chosen to be higher than the optimum value of $V_{\text{bias}} = (V_{Br} + V_p)/2$, as discussed previously [1]. In many practical situations, the source-to-drain voltage breakdown could occur before simultaneous gate–source and gate–drain voltage breakdown. Fig. 4(c) shows a shunt-mounted control MESFET. By arguments based as above, it can be seen that the positive-going cycle would limit the maximum channel current to I_{DSS} at low frequency. Finally, Fig. 4(d) shows a nonconducting-state MESFET, with the analysis similar to the series-mounted FET of Fig. 4(b).

TABLE I
CALCULATED VALUES OF R_c AND C_{nc} COMPARED WITH MEASURED VALUES (DEVICES FROM GUTMANN AND FRYKLUND [1])

DEVICE FROM REFERENCE [1]	R_c IN OHMS		C_{nc} IN PF	
	CALCULATED*	MEASURED	CALCULATED**	MEASURED
A	5.6 (55%)	5.5	.103 (85%)	.09
B	3.1 (42%)	4 0	.306 (84%)	.17
C	5.0 (46%)	7 5	085 (85%)	.07
D	5.9 (54%)	6.1	.083 (84%)	.09
E	2 2 (55%)	2 6	308 (83%)	.32
F	5.7 (53%)	6.6	.137 (82%)	.08
G	3.9 (51%)	4.2	.142 (85%)	.08

* Percentage contribution of R_{ch} in parenthesis, i.e R_{ch}/R_c
** Percentage contribution of C_{esd} in parenthesis, i.e. C_{esd}/C_{nc}

IV. RESULTS AND DISCUSSIONS

Experimental devices described in an earlier paper [1] have been used to benchmark these theoretical models. Typical source and drain metallization lengths were 40 μm and deep n^+-contact-to-metal pad separations were 1 μm, with the other dimensions presented previously by Gutmann and Fryklund [1]. The resistivity variation with doping followed Fukui's empirical resistivity formula [7]. Using the models developed in Section II, we calculated the resistances and the capacitances for the various devices, with C_{igs} and C_{igd} calculated at a bias voltage midway between pinch-off and breakdown.

The calculated and measured values of R_c and C_{nc} are given in Table I, along with the percentage contribution of R_{ch} and C_{esd}. In general, R_c values are close to those measured, while the modeled C_{nc} values are more than the measured values. We believe that proper accounting of the finite substrate thickness and the additional parasitic pad and crossover capacitances would result in closer agreement. From the modeled resistances and capacitances the cutoff-frequency figure of merit can be calculated using (1).

Next, we consider the dual 2-throw control component depicted in Fig. 5. In one of the states, the signal goes through the upper branch which is the low insertion loss state, while in the other state the signal is matched terminated in 50 Ω through the lower branch. The isolation and the insertion loss of the two states were calculated using the parameter values derived in Section II. The experimental and the theoretical results are displayed in Fig. 6, with excellent agreement being demonstrated.

The power handling capability of two control MESFET's in series in the low loss state was evaluated by measuring

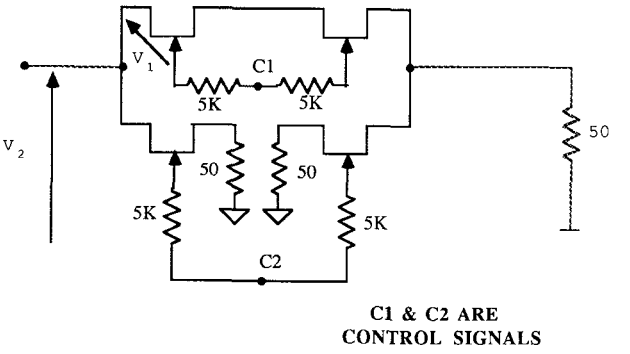
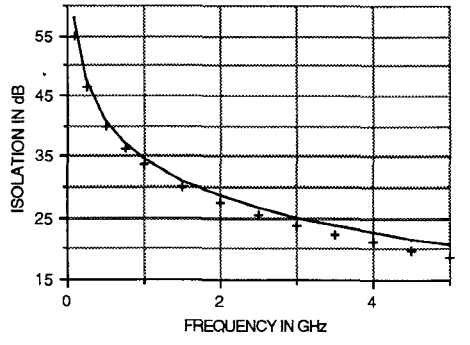


Fig. 5. The dual 2-throw control component.



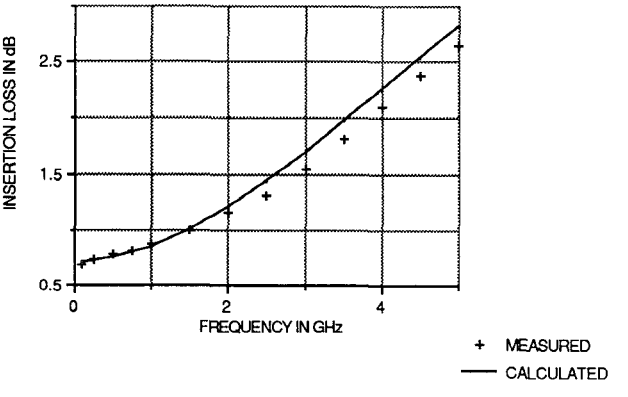


Fig. 6 Insertion loss and isolation versus frequency for the dual 2-throw component.

the input power for 1 dB compression versus frequency of the modified dual 2-throw component (with the 50 Ω termination in the lower branches removed) and is shown in Fig. 7. The varying power handling capability of the device with frequency results from the varying channel voltage that couples to the gate (through the gate-to-source/drain and gate-channel capacitances). In Fig. 7 we have also plotted the magnitude of the ratio of the RF gate-to-drain voltage (V_1 in Fig. 5) to the RF drain voltage (V_2 in Fig. 5). At frequencies of about 3 MHz or less the gate is effectively grounded through the bias resistance and, as a result, the positive-going channel cycle tends to pinch off the channel. At high frequencies (> 60 MHz), sufficient channel signal appears at the gate to increase the

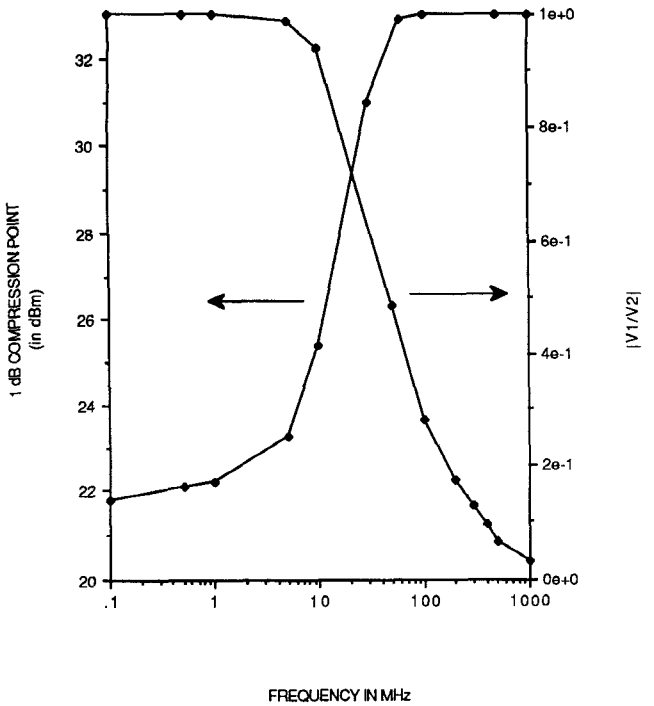


Fig. 7. Measured 1 dB compression point and calculated small-signal $|V_1/V_2|$ versus frequency for the modified dual 2-throw control component.

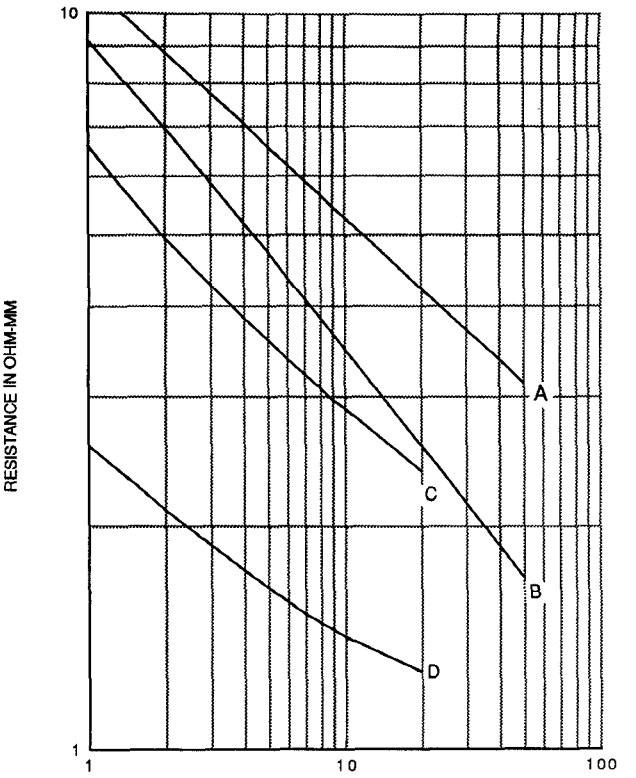


Fig. 8. Calculated conducting-state resistance for the various device structures.

power handling capability. The similarity of the two curves plotted in Fig. 7 supports the modeling assumptions.

V. Device Optimization and Future Trends

This section compares the devices shown in Fig. 1 from a perspective of optimizing the cutoff-frequency figure of merit. The length of the drain and source metal pads was assumed to be 40 μm, while the deep n^+ contact to metal pad was taken to be 1 μm. With these dimensions, the resistances of structures A–C were calculated at varying doping concentrations (from 1×10^{16} to 1×10^{18} cm^{-3}) and 3 V pinch-off voltage, with results shown in Fig. 8. At this point it should be noted that the approximation used in the Appendix overestimates the resistance when the channel doping concentrations are comparable to that of the n^+ surface region. Thus, the calculated resistances for structure C at high channel doping densities (i.e., 3×10^{17} cm^{-3} or more) are very approximate. To calculate the resistance of structure D the contact resistance as given by (13) was also included, with the results shown in Fig. 8. The significant contact resistance is dominated by the resistance of the deep n^+ contacts, assuming a realistic value of $R_{cc}W$ (0.025 $\Omega\cdot$mm).

The capacitances of the various structures were calculated at a bias voltage of one and a half times the pinch-off voltage. SAGFET devices with L'_{gs} and L'_{gd} much less than the channel height have lower breakdown voltages than conventional devices [8]. For such devices the bias voltage has to be between the pinch-off and breakdown voltages. However, we continue to use V_{bias} of one and a half times the pinch-off voltage even for the SAGFET's, which does not affect F_{cs} significantly.

From the calculated capacitances the cutoff-frequency figure of merit (F_{cs}) was calculated for devices with V_p of 3 V. Fig. 9 shows F_{cs} for the various structures as a function of doping. The SAGFET has a superior F_{cs}, with the maximum achievable value limited by the resistance of the deep n^+ contacts. However, the voltage handling capability of SAGFET is considerably inferior. To increase the breakdown voltage the n^+ deep contact to gate separation must be increased, indicating a trade-off between F_{cs} and voltage handling capability.

The upper bound in the F_{cs} with improvements in current technology was made by assuming 0.1 μm gate length, 0.1 μm gate to n^+ deep contact separation, 0.5 μm n^+ deep contact to metallization separation (resulting in a n^+ deep layer contact resistance of 0.26 $\Omega\cdot$mm), a drain and a source metallization of 5 μm, and a channel doping concentration of 5×10^{17} cm^{-3} for a 3 V pinch-off device to be 1340 GHz. Additional device fabrication and characterization are needed to evaluate the model validity in this region. As mentioned previously, the SAGFET for lowest conducting-state resistances has one key disadvantage: a reduced breakdown voltage which reduces its usefulness in other than low power applications.

VI. Conclusion

In this paper we have successfully modeled the key elements that determine the equivalent circuits for GaAs MESFET control devices for five device structures. The

broad-band cutoff-frequency figure of merit was calculated for some earlier reported devices, and the calculated values compared favorably with the experimental values. The broad-band cutoff-frequency figure of merit for the four devices in Fig. 1 was calculated with varying doping densities. The SAGFET was found to have the largest broad-band cutoff-frequency figure of merit, although it also has the least voltage handling capability. Further improvements in figure of merit critically depend upon contact resistance and maximum doping concentrations that can be achieved.

Future device miniaturization will result in broad-band cutoff-frequency figure of merits above 1000 GHz, allowing low power GaAs MESFET control devices to be utilized into the millimeter spectrum. Such high-frequency control devices compatible with MMIC implementations are very desirable for broad-band switching applications.

Appendix
Parasitic Resistance with n^+ Surface Layers

The parasitic resistance of device structure C can be approximated by a distributive resistive network of the type shown in Fig. 10. In this figure, r and R are the unit-length resistance of the n^+ and n regions respectively, and G is the conductance per unit length of the semiconductor region connecting r and R. These can be calculated using (9)–(11). Using the distributive network in Fig. 10, the following equations are obtained by applying Kirchhoff's law and solving for V_1, V_2, I_1, and I_2:

$$V_1 = \frac{1}{K^2}\left(Ae^{-Kl} + Be^{Kl}\right) + Cl + D \tag{A1}$$

$$I_1 = \frac{A}{Kr}e^{-Kl} - \frac{B}{Kr}e^{Kl} - \frac{C}{r} \tag{A2}$$

$$V_2 = \left(Ae^{-Kl} + Be^{Kl}\right)\left(\frac{1}{K^2} - \frac{1}{Gr}\right) + Cl + D \tag{A3}$$

$$I_2 = \frac{K}{R}\left(Ae^{-Kl} - Be^{Kl}\right)\left(\frac{1}{K^2} - \frac{1}{Gr}\right) - \frac{C}{R} \tag{A4}$$

where A, B, C, and D are boundary value dependent and K is given by (12).

For device structure C the boundary conditions can be applied (namely $I_2(0) = 0$, $I_1(L) = 0$, and $R_{p1} = (V_2(L) - V_1(0))/(I_1 + I_2)$, and the resistance of the distributive resistive network is obtained as

$$R_{p1} = \frac{r\|R}{K}\left[\left(\frac{r}{R} + \frac{R}{r}\right)\coth KL + \frac{2}{\sinh KL}\right] + L(r\|R) \tag{A5}$$

where L is the length of the region (i.e., either L'_{gs} as in Fig. 10 or L'_{gd}). At this point it is important to note that in this analysis we have assumed that the resistance r is much smaller than R. This approximation is invalid at high channel doping concentrations.

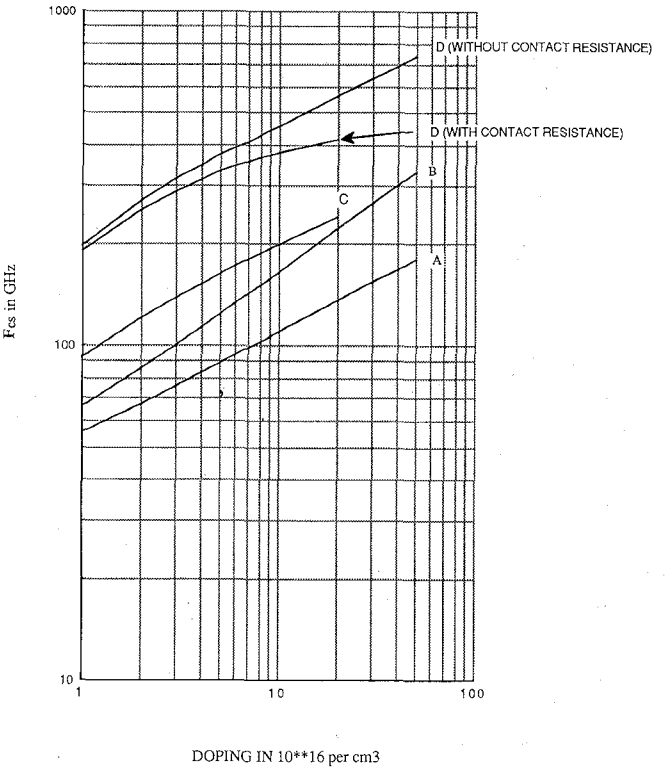


Fig. 9. Cut-off frequency figure of merit for 3 V pinch-off devices.

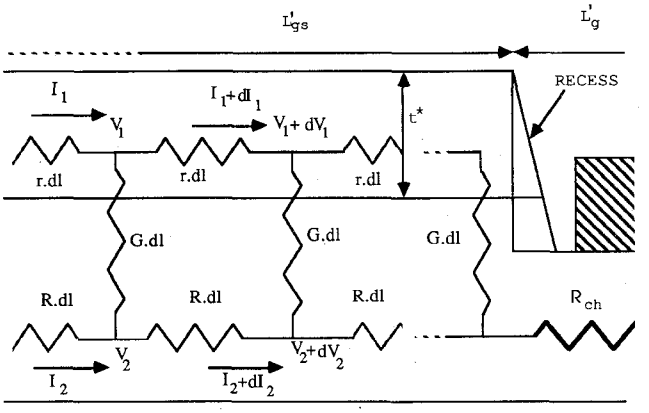


Fig. 10. The distributive resistive network used to calculate the parasitic resistance of device structure C.

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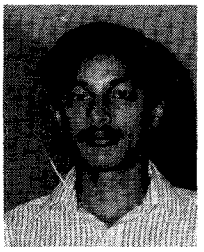

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